

FIG. 1

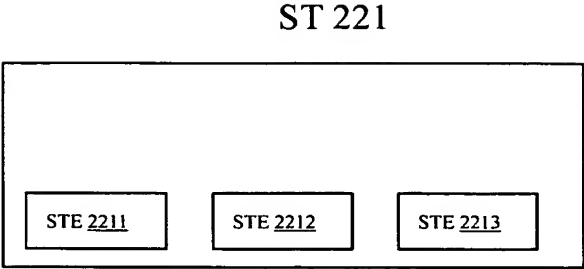


FIG. 3

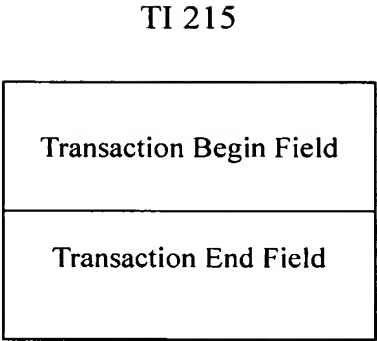


FIG. 4a

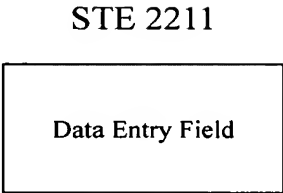


FIG. 4b

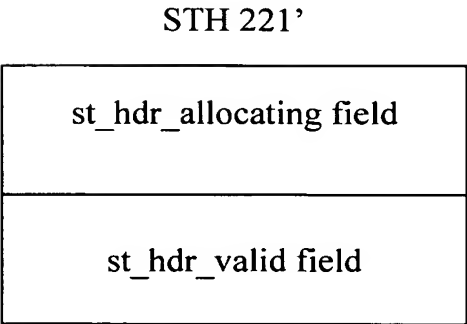


FIG. 4c

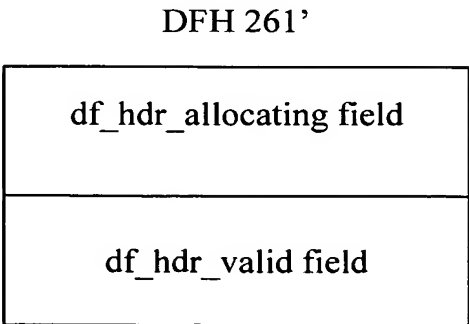


FIG. 4d

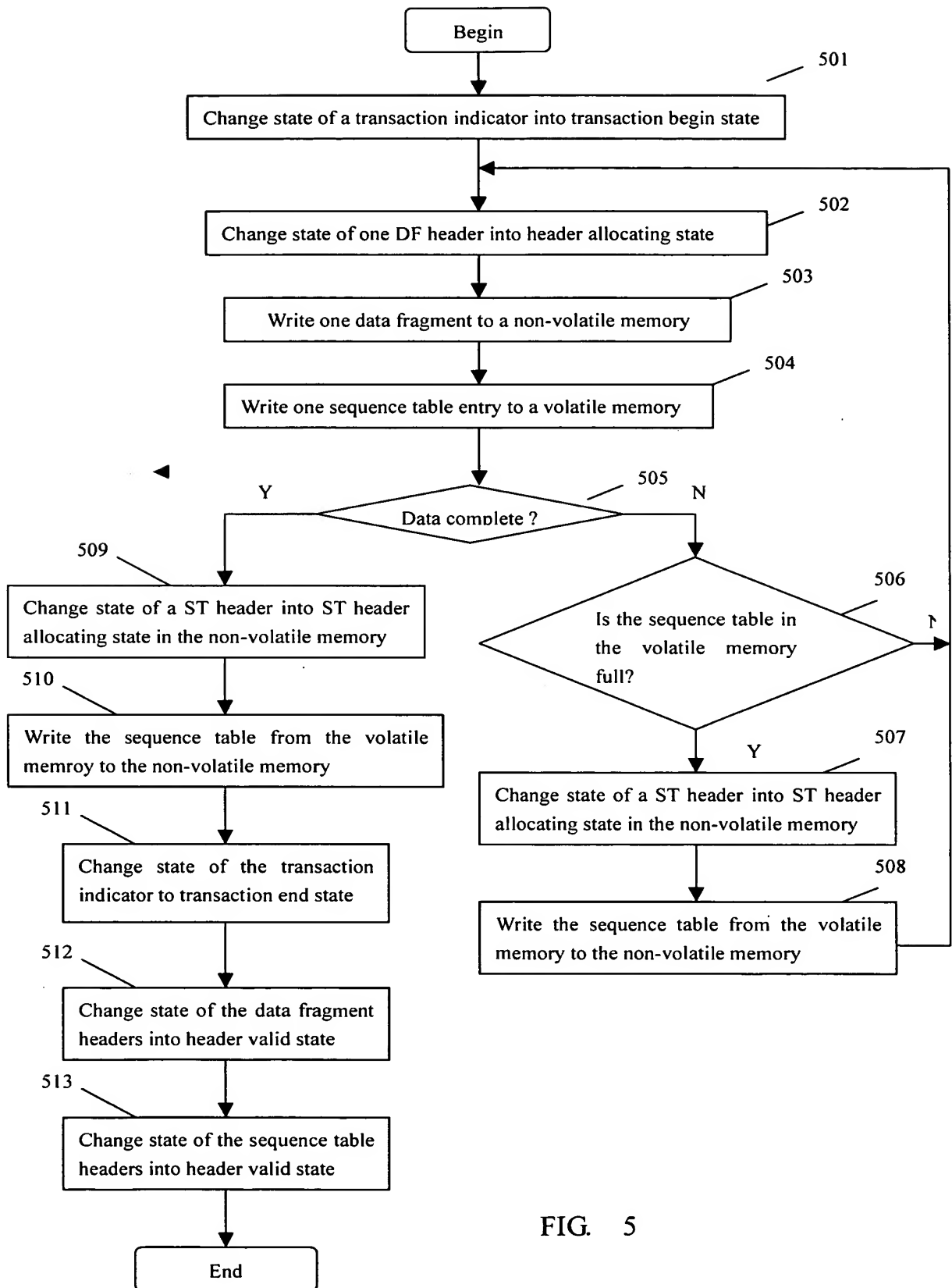


FIG. 5

	Sequence Table	Data Fragment	Write Mode
1		hdr_allocating (1)	1 Bit Twiddling
2		Data Fragment (1)	1 KB Buffer Programming
3	hdr_allocating		1 Bit Twiddling
4	entry_allocating (1)		1 Bit Twiddling
5	data entry (1)		2 Words Programming
6	entry_valid (1)		1 Bit Twiddling
7		hdr_valid (1)	1 Bit Twiddling
8
9		hdr_allocating (64)	1 Bit Twiddling
10		Data Fragment (64)	1 KB Buffer Programming
11	entry_allocating (64)		1 Bit Twiddling
12	data entry (64)		2 Words Programming
13	entry_valid (64)		1 Bit Twiddling
14	hdr_valid		1 Bit Twiddling
15		hdr_valid (64)	1 Bit Twiddling

Bit twiddling (bits)	258
word program (words)	128
Buffer program (bytes)	64K

	Sequence Table	Data Fragment	Write Mode
1	transaction begin		1 Bit Twiddling
2		hdr_allocating (1)	1 Bit Twiddling
3		Data Fragment (1)	1 KB Buffer Programming
4	
5		hdr_allocating (64)	1 Bit Twiddling
6		Data Fragment (64)	1 KB Buffer Programming
7	hdr_allocating		1 Bit Twiddling
8	data entries		0.5KB Buffer Programming
9	transaction end		1 Bit Twiddling
10		hdr_valid (1)	1 Bit Twiddling
11	
12		hdr_valid (64)	1 Bit Twiddling
13	hdr_valid		1 Bit Twiddling
14			

Bit twiddling (bits)	132
word program (words)	0
Buffer program (bytes)	64.5K

Fig. 6

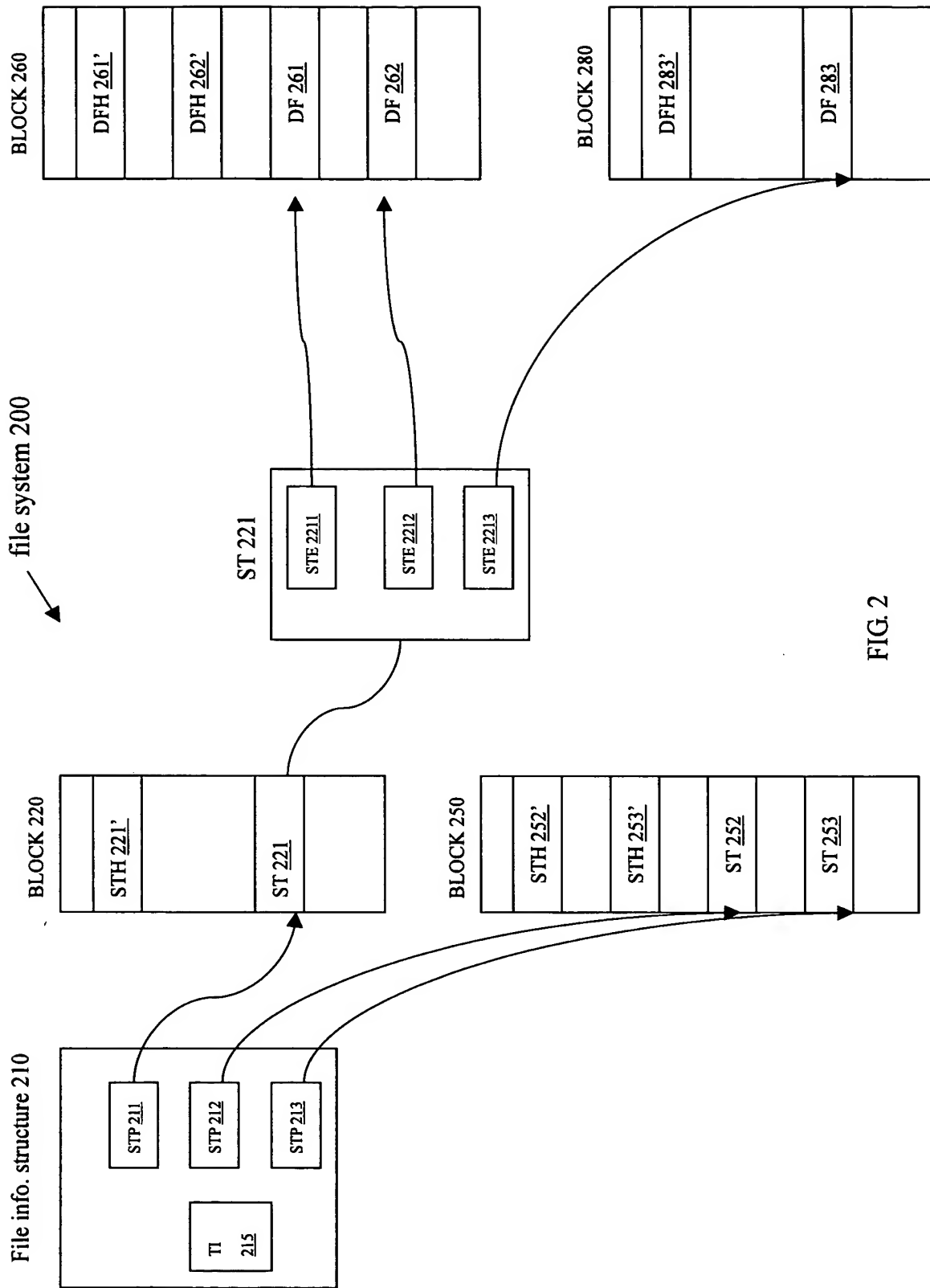


FIG 2